What is Claimed is:

1. A compensated amplifier, for amplifying an input signal applied to an input node to provide an output signal at an amplifier output node, comprising:

a first amplifier stage having an internal node as an input thereto and having a first stage output node;

a second amplifier stage coupled to said first amplifier stage, having said input node as an input thereto and providing said output signal at said amplifier output node; and

a capacitor coupled between said output node and said internal node.

2. A compensated amplifier according to Claim 1, wherein said second amplifier stage is coupled to said first amplifier stage such that said first stage output node is common with said amplifier output node.

3. A compensated amplifier according to Claim 1, wherein said second amplifier stage is coupled to said first amplifier stage such that said first stage output node is connected to said input node.

4. A compensated amplifier according to Claim 1, wherein said capacitor is connected such that a left-hand-plane zero is provided in said compensated amplifier.

5. A compensated amplifier according to Claim 4, wherein said left-hand-plane zero is selected so as to optimize compensation for said compensated amplifier.

6. A compensated amplifier according to Claim 1, wherein said first amplifier stage comprises a bipolar transistor current mirror.

7. A compensated amplifier according to Claim 1, wherein, in operation, capacitive current flows through said capacitor, and said capacitive current is sensed at said internal node and amplified by said first amplifier stage.

8. A compensated amplifier according to Claim 7, wherein said first amplifier stage comprises a diode connected transistor and a ratioed transistor connected together forming a current mirror, and wherein said diode connected transistor senses said capacitive current at said internal node and said ratioed transistor amplifies said capacitive current.

9. A Miller-compensated amplifier, for amplifying an input signal applied to an amplifier input node to provide an output signal at an amplifier output node, comprising:

a first amplifier stage having an internal node as an input thereto, and having a first stage output node;

a second amplifier stage having said amplifier input node as an input thereto, and having a second stage output node;

a third amplifier stage having a third stage input node coupled to said first stage output node and to said second stage output node, and providing said output signal at said amplifier output node; and

a capacitor coupled between said amplifier output node and said internal node.